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9. United States patent application serial no. 09/204,479 entitled, "Implicitly Derived Register Specifiers in a Processor", naming Marc Tremblay and William Joy as inventors and filed on December 3, 1998.

In the Drawings

Kindly replace the original drawings with the attached formal drawings.

In the Claims

Kindly cancel all claims in the parent application and add new claims 1-5, as follows:

Rule 1.126 Sub 61

29 1. A context switch controller in a processor that includes an operand data storage for holding data operated upon by instructions executing on the processor, the operand data storage being divided into a plurality of storage groups containing one or more storage elements, the context switch controller comprising:

a dirty bit storage including one or more storage bits that correspond to one or more respective storage groups in the operand data storage; and

A1 a dirty bit logic coupled to the dirty bit storage and coupled to receive a destination address field of the instructions, the dirty bit logic responsive to an executed instruction by classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction and by evaluating the classified destination based on whether the instruction updates the targeted storage group.

30 2. A context switch controller according to Claim 29 wherein:

the dirty bit logic is responsive to a context switch by saving storage groups based on the evaluation of the classified destinations.

31 3. A processor comprising:

a plurality of functional units;

a register file including a plurality of register file segments coupled to and associated with the plurality of functional units, respectively, the register file being divided into a plurality of register groups;

a dirty bit register coupled to the register file; and

means coupled to the dirty bit register for accessing a destination register (rd) field of an instruction;

means for classifying the destination register rd according to the address in the rd field, the classification corresponding to a bit in the dirty bit register; and

means for evaluating the dirty bit register to designate that the particular classification includes a register that is written by the instruction.

4. A processor according to Claim 3 further comprising:

means coupled to the dirty bit register and coupled to the register file for storing a plurality of dirty bits designating enablement or disablement of access to the register file on a register group-by-register group basis; and

means responsive to an instruction that accesses the register file for determining whether access is enabled by the dirty bit of the dirty bit enable register corresponding to the register group of the register file accessed by the instruction, permitting access if access is enabled.

5. A context switching logic in a processor that includes an executive storage for holding operand data operated upon by instructions executing on the processor, the executive storage being divided into a plurality of storage groups containing one or more storage elements, the context switching logic comprising:

means for utilizing a dirty bit storage including a plurality of storage bits corresponding to a plurality of respective storage groups in the executive storage;

means for receiving a destination address field of the executing instructions;

means for responsive to an executed instruction, classifying a destination access as a targeted storage group according to information in the destination address field of the executed instruction;

means for evaluating the classified destination based on whether the instruction updates the targeted storage group; and